STI Forming Method for Improving STI Step Uniformity

BACKGROUND OF THE INVENTION

1.Field of the Invention

This invention relates to a process for shallow trench isolation (STI) in a semiconductor structure, more specifically, to a method for improving the STI step uniformity.

2. Description of the Prior Art

In the manufacturing process for semiconductor integrated circuits such as DRAMs, shallow trench isolations (STI) are often used to isolate the respective elements.

Generally, in the semiconductor device such as a DRAM, a pad oxide layer with a thickness of about tens angstrom is deposited on a substrate, and then a pad nitride layer, of which the material can be SiN, with a thickness of about a thousand angstrom above is deposited on the pad oxide layer. The intermediate structure having the substrate, the pad oxide layer and the pad nitride layer is subject to steps of photo-mask developing, etching and removing the mask and the like to form shallow trench isolations. The formation of STIs separate active regions of the semiconductor structure.

With reference to Fig. 1, a structure in shown with STIs 20 and 21 formed. In this drawing, the reference numbers 10 and 11 indicate substrate, 12 and 13 indicate pad oxide layers, 14 and 15 indicate pad nitride layers. As shown, in the whole semiconductor device structure, a phenomenon that the STIs 20 and 21 in different regions have different depths is likely to happen.

With reference to Fig. 2, under the situation that the depths of STIs 20 and 21 are not uniform, when using high density plasma (HDP), for example, to form an oxide layer 30 on the whole structure, the overfill thickness t of the oxide at the region of the shallow STI 20 will be thicker than that at the region of the deep STI 21.

Then, the oxide layer 30 is planarized by chemical mechanical polishing (CMP). The height difference between the top of the planarized oxide layer 30 and the top of the substrate of the active region is referred to STI step. As can be seen from Fig. 3, since the overfill thicknesses of the oxide are different, after planarization, the STI steps in the regions of STIs of different depths are different. As shown in the right part of Fig. 3, it is possible that the nitride layer 15 is partially removed in the polishing step.

In the process for DRAM, the active regions separated from each other by the STIs will have gates or bit lines formed thereon. Generally, in DRAM structure, the non-uniformity of

the STI steps is likely to cause gate stringer, thereby causing improper short circuit between the gates or between the gate and bit line.

Therefore, a solution to solve the above problems is necessary. The present invention satisfies such a need.

SUMMARY OF THE INVENTION

An objective of the present invention is to provide a STI forming method, which can improve the uniformity of STI steps.

According to an aspect of the present invention, a STI forming method for improving STI step uniformity has the steps of depositing an oxide layer on a semiconductor structure formed with STIs, and forming a planarizing material layer on the oxide layer, then performing chemical mechanical polishing process.

According to another aspect of the present invention, in the STI forming method for improving STI step uniformity, the material of the planarizing material layer is boron phosphorus silicate glass (BPSG), and is subject to heat reflow process.

According to a further aspect of the present invention, in the STI forming method for improving STI step uniformity, the material of the planarizing material layer is anti-reflective material.

BRIEF DESCRIPTION OF THE DRAWINGS

The following drawings are only for illustrating the mutual relationships between the respective portions and are not drawn according to practical dimensions and ratios. In addition, the like reference numbers indicate the similar elements.

Fig. 1 shows a prior art semiconductor device structure having shallow trench isolations formed therein;

Fig. 2 shows the structure of Fig. 1 having an oxide layer formed thereon;

Fig. 3 shows a structure obtained by having the structure of Fig. 2 subjected to CMP;

Fig. 4 shows a structure obtained by having a planarizing material layer formed on the structure of Fig. 2 in accordance with the present invention; and

Fig. 5 shows a structure obtained by having the structure of Fig. 4 subjected to CMP.

DETIALED DESCRIPTION OF THE PREFERRED EMBODIMENT

The technical contents, objectives and achieved effects of the present invention will be described further in detail with the following embodiment.

First of all, forming shallow trench isolations to separate the respective active areas in the semiconductor structure according to known process, as shown in Fig. 1. Then, with reference to Fig. 2, applying oxide to form an oxide layer 30 on the structure having the shallow trench isolations formed therein to cover the entire structure and fill within the respective shallow trench isolations.

Before performing chemical mechanical polishing (CMP), a planarizing material layer 40 is deposited on the oxide layer 30, as shown in Fig. 4. The planarizing material layer 40 may use BPSG, and is heated to make the BPSG reflow, so as to achieve planarization. Alternatively, the planarizing material layer 40 may use anti-reflective material. Since the anti-reflective material is in flowable condition at a common operational temperature, so that planarization can be achieved. Although only these two materials are mentioned above, any proper material which is flowable under a certain condition to achieve the goal of planarization can be also used.

Subsequently, chemical mechanical polishing (CMP) or any other proper polishing is performed to polish off the planarization material layer 40 and a portion of the oxide layer 30, and the obtained structure is shown in Fig. 5. As can be seen in the drawing, the heights of the STI steps at the shallow STI region and the deep STI region are uniform.

The formation of the planarization material layer 40 makes the uniformity of STI step lifted after CMP process, thereby solving the problems of STI step non-uniformity in prior art.

While the embodiment of the present invention is illustrated and described, various modifications and alterations can be made by persons skilled in this art. The embodiment of the present invention is therefore described in an illustrative but not restrictive sense. It is intended that the present invention may not be limited to the particular forms as illustrated, and that all modifications and alterations which maintain the spirit and realm of the present invention are within the scope as defined in the appended claims.